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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/016,194	11/02/2001	Ketankumar B. Patel	01CON231P	4343

25700 7590 02/20/2004

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EXAMINER	
BRINEY III, WALTER F	
ART UNIT	**PAPER NUMBER**
2644	6

DATE MAILED: 02/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/016,194	PATEL, KETANKUMAR B.	
	Examiner	Art Unit	
	Walter F Briney III	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 4 and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "**is greater than**" in claim 4 is a relative term which renders the claim indefinite. The term "**is greater than**" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Claim 4 is limited to **the DC driver circuit of claim 3, wherein said first capacitor is greater than said second capacitor**. Said first capacitor has to be greater than a second capacitor, but the disclosure presents no way to measure the range that encapsulates said second capacitor value. See ex parte Brummer, 12 USPQ2d 1653 (Bd. Pat. App. & Inter. 1989).

Claim 18 is essentially the same as claim 4 and is rejected for the same reasons.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 5, 6, 8, 10-17, 20, and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Okada (US Patent 5,425,096).

Claim 1 is limited to **a DC driver circuit coupled to a tip/ring line**. Okada discloses a pulse dialer circuit with a **first capacitor** (figure 2, element C2) **coupled to** a first transistor (i.e. **a first switch**) (figure 2, element 95). The switch is coupled to a second transistor (i.e. **an amplification circuit**) (figure 2, element 93). The second transistor is coupled between a **tip/ring line** (figure 2, output of diode bridge). Okada further discloses a **RC circuit** (figure 2, elements C1 and R4) coupled to a third transistor (i.e. **a second switch**) (figure 2, element 94). Again, the third transistor is coupled to the second transistor (i.e. **said second switch coupled to said amplification circuit**). A CPU causes the third transistor (i.e. **second switch**) to **close** during a **make state** of the pulse dialer. This causes the potential at node D (figure 2) to rise because the amplifier is drawing current from the tip/ring line. When the voltage reaches that of the tip/ring line, the first transistor (i.e. **first switch**) **closes** (i.e. **said first switch being closed and said second switch being closed during a make state**). The second amplifier is thus **opened** to allow current to pass (i.e. **to cause said amplification circuit to draw current from said tip/ring line**). Conversely when in a **break state** of the pulse dialer, the CPU disables (i.e. **opens**) the third transistor, which causes the charge at node D to eventually dissipate, thus **opening** the first transistor (i.e. **said first switch being open and said second switch being open during a**

break state to prevent said amplification circuit from drawing current from said tip/ring line). Therefore, Okada anticipates all limitations of the claim.

Claim 3 is limited to **the DC driver circuit of claim 1**, as covered by Okada. Okada discloses a **said RC circuit** with a resistor and a **second capacitor** (figure 2, element C1). The capacitor is connected to the second transistor (i.e. **amplification circuit**) (figure 2, element 94) and the negative output of the polarity guard (i.e. **ground**). Therefore, Okada anticipates all limitations of the claim.

Claim 17 is essentially the same as claim 3 and is rejected for the same reasons.

Claim 5 is limited to **the DC driver circuit of claim 1**, as covered by Okada. Okada discloses a **RC circuit** with a **resistor** (figure 2, element R4). The resistor is connected to the second transistor (i.e. **amplification circuit**) (figure 2, element 94) and the negative output of the polarity guard (i.e. **ground**). Therefore, Okada anticipates all limitations of the claim.

Claim 20 is essentially the same as claim 5 and is rejected for the same reasons.

Claim 6 is limited to **the DC driver circuit of claim 1**, as covered by Okada. Okada discloses a third transistor (i.e. **an op amp**) (figure 2, element 94) coupled to a second transistor (i.e. **first transistor**) (figure 2, element 93). Therefore, Okada anticipates all limitations of the claim.

Claim 8 is limited to **the DC driver circuit of claim 6**, as covered by Okada. Okada discloses enabling (i.e. **opening**) the second transistor (i.e. **said first transistor**) (figure 2, element 93) to draw current when in a **make state** and disabling it during a **break state**. Therefore, Okada anticipates all limitations of the claim.

Claim 10 is limited to **the DC driver circuit of claim 1**, as covered by Okada. Okada discloses a pulse dialing circuit that is further coupled to a modem (i.e. **wherein said tip/ring line is coupled to a modem**) (figure 2, see MODEM SIDE). Therefore, Okada anticipates all limitations of the claim.

Claim 21 is essentially the same as claim 10 and is rejected for the same reasons.

Claim 11 is limited to **a circuit for reducing a peak voltage at a selected line**. Okada discloses a first transistor (i.e. **at least one transistor**) (figure 2, element 93) that transmits pulses on the tip/ring line (i.e. **driving said selected line**). Okada discloses a **first capacitor** (figure 2, element C2). The first capacitor holds the DC voltage across the tip/ring pair when the first transistor is closed (i.e. **circuit is in a make state**), where the voltage held across the tip/ring line is fed-back to the input of the first transistor through resistor R1 (i.e. **said at least one transistor being driven by a first capacitor when said circuit is in a make state**). The first transistor is opened during a **break state** after a second transistor opens (figure 2, element 94), the rate at which the second transistor opens is based on a RC circuit (i.e. **said at least one transistor being driven by an RC circuit when said circuit is in a break state**). The RC circuit has a tip/ring input, and by the nature of an RC circuit it **reduces said peak voltage at said selected line when said circuit transitions from said make state to said break state**. Therefore, Okada anticipates all limitations of the claim.

Claim 12 is limited to **the circuit of claim 11**, as covered by Okada. Okada discloses connecting the dial pulse circuit to a **tip/ring pair** (figure 2, see TELEPHONE LINE SIDE). Therefore, Okada anticipates all limitations of the claim.

Claim 13 is limited to **the circuit of claim 11**, as covered by Okada. The first transistor (i.e. **said at least one transistor) is driven by** a second transistor (i.e. **op amp**) (figure 2, element 94). Therefore, Okada anticipates all limitations of the claim.

Claim 14 is limited to **the circuit of claim 13**, as covered by Okada. Okada discloses a second transistor (i.e. **op amp**) that has an input from the tip/ring pair, which is held at a steady DC value by the **first capacitor** when the first transistor is closed (i.e. **during a make state**). Therefore, Okada anticipates all limitations of the claim.

Claim 15 is limited to **the circuit of claim 11**, as covered by Okada. Okada discloses a third transistor (i.e. **first switch**) (figure 2, element 95). The third transistor uses charge in the **first capacitor** to hold the line voltage when the DC loop is closed (i.e. **make state**), thus providing a certain DC value on the telephone line that is fed into the first transistor (i.e. **at least one transistor**) via R1 (i.e. **wherein a first switch causes said at least one transistor to be driven by said first capacitor when said circuit is in said make state**). Therefore, Okada anticipates all limitations of the claim.

Claim 16 is limited to **the circuit of claim 15**, as covered by Okada. Okada discloses a fourth transistor (i.e. **a second switch**) (figure 2, element 91) that controls the voltage at node A, which controls the second transistor (i.e. **op-amp**) (figure 2, element 94), which controls the first transistor (i.e. **at least one transistor**) (figure 2, element 93). The rate at which the first transistor reacts to the fourth transistor while

switching to the **break state** is defined by capacitor C1 and resistor R4 (i.e. **wherein a second switch causes said at least one transistor to be driven by said RC circuit when said circuit is in said break state**). Therefore, Okada anticipates all limitations of the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okada in view of Fischer et al. (US Patent 6,621,904).

Claim 2 is limited to **the DC driver circuit of claim 1**, as covered by Okada. Okada discloses a fourth transistor (i.e. **a third switch**) (figure 2, element 92) coupled to the **first capacitor** (figure 2, element C2). When in the **break state**, the switch is closed prior to going to the **make state** to minimize the switching delays. However, this changes the effective impedance of the circuit, which is known to cause signal reflections. Therefore, Okada anticipates all limitations of the claim with the exception of **precharging said first capacitor**. Fischer teaches minimizing the time spent in charging capacitors used in DC setup by precharging the capacitors with a power source coupled between a switch and a capacitor (figure 3, element S2). It would have been obvious to one of ordinary skill in the art at the time of the invention to precharge

the DC setup capacitor as taught by Fischer for the purpose of avoiding signal reflections that can occur due to changing the impedance of the DC hold circuit.

Claim 19 is essentially the same as claim 2 and is rejected for the same reasons.

Claims 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okada in view of Reichelt (US Patent 5,121,425).

Claim 7 is essentially the same as claim 6, as covered by Okada. Therefore, Okada anticipates all limitations of the claim with the exception of **said first transistor being coupled to a second transistor**. Reichelt teaches that Darlington pair transistors are superior for pulse dialing applications because their high current gains decrease the amount of loss (figure 4, element DT) (column 4, lines 46-60). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use Darlington pair transistors as taught by Reichelt for the purpose of creating a dial pulse circuit with high gain and low loss.

Claim 9 is limited to **the DC driver circuit of claim 7**, as covered by Okada in view of Reichelt. The operation of the Darlington pair transistors would be identical to the operation of a single transistor as originally disclosed by Okada. Therefore, claim 9 is essentially the same as claim 8 and is rejected for the same reasons.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter F Briney III whose telephone number is 703-305-0347. The examiner can normally be reached on M-F 8am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Forester W Isen can be reached on 703-305-4386. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WFB
2/17/04

MINSUN CHARVEY
PRIMARY EXAMINER